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What is claimed is:

1. A semiconductor integrated circuit device comprising:

a plurality of first field effect transistors constituting a memory cell of an SRAM and provided on a semiconductor substrate; and

second field effect transistors other than said first field effect transistors provided on said semiconductor substrate,

wherein the threshold voltage of at least one first field effect transistor among said plurality of first field effect transistors is relatively higher than the threshold voltage of said second field effect transistor.

2. A semiconductor integrated circuit device comprising a driving field effect transistor, a transfer field effect transistor and a load field effect transistor constituting a memory cell of an SRAM and provided on a semiconductor substrate; and

another field effect transistor provided on said semiconductor integrated circuit,

wherein the threshold voltage of at least two of or all of said driving field effect transistor, transfer field effect transistor or load field effect transistor is relatively higher than the threshold

voltage of said other field effect transistor.

3. A semiconductor integrated circuit device comprising a driving field effect transistor constituting a memory cell of an SRAM and provided on a semiconductor substrate; and

another field effect transistor provided on said semiconductor substrate,

wherein the threshold voltage of said transfer field effect transistor is relatively higher than the threshold voltage of said other field effect transistor.

4. A semiconductor integrated circuit device comprising a driving field effect transistor constituting a memory cell of an SRAM and provided on a semiconductor substrate; and

another field effect transistor provided on said semiconductor substrate,

wherein the threshold voltage of said transfer field effect transistor is relatively higher than the threshold voltage of said other field effect transistor with a designed thickness of a gate insulation film of said transfer field effect transistor being the same as a designed thickness of a gate insulation film of said other field effect transistor.

5. A semiconductor integrated circuit device comprising a load field effect transistor constituting a memory cell of an SRAM and provided on a semiconductor substrate; and

another field effect transistor provided on said semiconductor substrate,

wherein the threshold voltage of said load field effect transistor is relatively higher than the threshold voltage of said other field effect transistor.

6. A semiconductor integrated circuit device according to Claim 1, wherein the operating speed thereof is 100 MHz or more.

7. A semiconductor integrated circuit device according to Claim 1, wherein an isolation portion provided on said semiconductor substrate has a groove type structure.

8. A semiconductor integrated circuit device according to Claim 1, wherein a designed channel width of at least one of said first field effect transistor is smaller than a designed channel width of said second field effect transistor.

9. A method for manufacturing a semiconductor integrated circuit device having a plurality of first field effect transistors constituting a memory cell of

an SRAM and second field effect transistor other than them formed on a semiconductor substrate, comprising:

an impurity introduction step for selectively introducing a first impurity into a region to form at least one of said first field effect transistors on said semiconductor substrate in order to set the threshold voltage of said at least one first field effect transistor among said plurality of first field effect transistors relatively higher than the threshold voltage of said second field effect transistor.

10. A method for manufacturing a semiconductor integrated circuit device having a plurality of first field effect transistors constituting a memory cell of an SRAM and second field effect transistors other than them formed on a semiconductor substrate, which comprising:

(a) a step of forming a groove on said semiconductor substrate;

(b) an impurity introduction step for selectively introducing a first impurity into a region to form at least one of said first field effect transistors on said semiconductor substrate in order to set the threshold voltage of said at least one first field effect transistor among said plurality of

first field effect transistors relatively higher than the threshold voltage of said second field effect transistor;

(c) a step of forming an isolation portion by burying an insulation film in said groove after said step (b); and

(d) an impurity introduction step for selectively introducing a second impurity into a region to form field effect transistors of the same conductivity type on said semiconductor substrate in order to set the threshold voltage of said second field effect transistor, after said step (c).

11. A method for manufacturing a semiconductor integrated circuit device having a plurality of first field effect transistors constituting a memory cell of an SRAM and second field effect transistors other than them formed on a semiconductor substrate, which comprising:

(a) a step of forming a groove on said semiconductor substrate;

(b) a step of forming an isolation portion by burying an insulation film in said groove after said step of forming a groove;

(c) an impurity introduction step for selectively introducing a first impurity into a region

to form at least one of said first field effect transistors on said semiconductor substrate in order to set the threshold voltage of said at least one first field effect transistor among said plurality of first field effect transistors relatively higher than the threshold voltage of said second field effect transistor, after said step (b); and

(d) an impurity introduction step for selectively introducing a second impurity into a region to form field effect transistors of the same conductivity type on said semiconductor substrate in order to set the threshold voltage of said second field effect transistor, after said step (c).

12. A method for manufacturing a semiconductor integrated circuit device according to Claim 9, wherein said at least one field effect transistor is a driving field effect transistor.

13. A method for manufacturing a semiconductor integrated circuit device having a plurality of first field effect transistors constituting a memory cell of an SRAM and second field effect transistor other than them formed on a semiconductor substrate, which comprising:

(a) a step of forming a gate insulation film on said semiconductor substrate;

(b) a step of forming a photoresist pattern on the semiconductor substrate after said step (a) to cover the regions to form said first field effect transistors and to expose other regions, and thereafter removing the gate insulation film exposed by the same used as a mask; and

(c) a step of removing said photoresist pattern after said step (b) and thereafter performing an oxidation process on said semiconductor substrate to form, in the regions to form said first field effect transistors, a gate insulation film thicker than a gate insulation film formed in the region to form said second field effect transistor,

thereby setting the threshold voltage of at least one first field effect transistor among said plurality of first field effect transistors relatively higher than the threshold voltage of said second field effect transistor.

14. A method for manufacturing a semiconductor integrated circuit device having a first field effect transistor constituting a memory cell of an SRAM and a second field effect transistor other than it formed on a semiconductor substrate, which comprising:

(a) a step of selectively introducing a first impurity into the region to form said at least one

first field effect transistor on said semiconductor substrate; and

(b) a step of forming, in the region to form said at least first field effect transistor, a gate insulation film thicker than a gate insulation film formed in the region to form said second field effect transistor, on said semiconductor substrate, thereby setting the threshold voltage of at least one first field effect transistor among said plurality of first field effect transistors relatively higher than the threshold voltage of said second field effect transistor.

15. A method for manufacturing a semiconductor integrated circuit device having a plurality of first field effect transistors constituting a memory cell of an SRAM and second field effect transistor other than them formed on a semiconductor substrate, which comprising:

(a) a step of forming a groove on said semiconductor substrate;

(b) an impurity introduction step for selectively introducing a first impurity into a region to form at least one of said first field effect transistors on said semiconductor substrate in order to set the threshold voltage of said at least one

first field effect transistor among said plurality of first field effect transistors relatively higher than the threshold voltage of said second field effect transistor, after said step (a);

(c) a step of forming an isolation portion by burying an insulation film in said groove after said step of forming a groove after said step (b);

(d) an impurity introduction step for selectively introducing a second impurity into a region to form field effect transistors of the same conductivity type on said semiconductor substrate in order to set the threshold voltage of said second field effect transistor, after said step (c);

(e) a step of forming a gate insulation film on the semiconductor substrate after said step (d);

(f) a step of forming a photoresist pattern on the semiconductor substrate after said step (e) to cover the regions to form said first field effect transistors and to expose other regions, and thereafter removing the gate insulation film exposed by the same used as a mask; and

(g) a step of removing said photoresist pattern after said step (f) and thereafter performing an oxidation process on said semiconductor substrate to form, in the regions to form said first field effect

transistors, a gate insulation film thicker than a gate insulation film formed in the region to form said second field effect transistor.

16. A method for manufacturing a semiconductor integrated circuit device having a plurality of first field effect transistors constituting a memory cell of an SRAM and a second field effect transistor other than them formed on a semiconductor substrate, which comprising:

(a) a step of forming a groove on said semiconductor substrate;

(b) a step of forming an isolation portion by burying an insulation film in said groove after said step of forming a groove;

(c) an impurity introduction step for selectively introducing a first impurity into a region to form at least one of said first field effect transistors on said semiconductor substrate in order to set the threshold voltage of said at least one first field effect transistor among said plurality of first field effect transistors relatively higher than the threshold voltage of said second field effect transistor, after said step (b);

(d) an impurity introduction step for selectively introducing a second impurity into a

region to form field effect transistors of the same conductivity type on said semiconductor substrate in order to set the threshold voltage of said second field effect transistor, after said step (b);

(e) a step of forming a gate insulation film on the semiconductor substrate after said step (d);

(f) a step of forming a photoresist pattern on the semiconductor substrate after said step (e) to cover the regions to form said first field effect transistors and to expose other regions, and thereafter removing the gate insulation film exposed by the same used as a mask; and

(g) a step of removing said photoresist pattern after said step (f) and thereafter performing an oxidation process on said semiconductor substrate to form, in the regions to form said first field effect transistors, a gate insulation film thicker than a gate insulation film formed in the region to form said second field effect transistor.

17. A method for manufacturing a semiconductor integrated circuit device having a plurality of first field effect transistors constituting a memory cell of an SRAM and second field effect transistor other than them formed on a semiconductor substrate, which comprising:

a step of selectively introducing nitrogen into the region to form said second field effect transistor on said semiconductor substrate and thereafter forming a gate insulation film on said semiconductor substrate,

thereby setting the threshold voltage of at least one first field effect transistor among said plurality of first field effect transistors relatively higher than the threshold voltage of said second field effect transistor.

18. A method for manufacturing a semiconductor integrated circuit device having a plurality of first field effect transistors constituting a memory cell of an SRAM and second field effect transistor other than them formed on a semiconductor substrate, which comprising:

(a) a step of selectively introducing a first impurity into the region to form said at least one first field effect transistor on said semiconductor substrate; and

(b) a step of selectively introducing nitrogen into the region to form said second field effect transistor on said semiconductor substrate and thereafter forming a gate insulation film on said semiconductor substrate,

thereby setting the threshold voltage of at least one first field effect transistor among said plurality of first field effect transistors relatively higher than the threshold voltage of said second field effect transistor.

19. A method for manufacturing a semiconductor integrated circuit device having a plurality of first field effect transistors constituting a memory cell of an SRAM and second field effect transistor other than them formed on a semiconductor substrate, which comprising:

(a) a step of forming a groove on said semiconductor substrate;

(b) an impurity introduction step for selectively introducing a first impurity into a region to form at least one of said first field effect transistors on said semiconductor substrate in order to set the threshold voltage of said at least one first field effect transistor among said plurality of first field effect transistors relatively higher than the threshold voltage of said second field effect transistor, after said step (a);

(c) a step of forming an isolation portion by burying an insulation film in said groove after said step of forming a groove after said step (b);

(d) an impurity introduction step for selectively introducing a second impurity into a region to form field effect transistors of the same conductivity type on said semiconductor substrate in order to set the threshold voltage of said second field effect transistor, after said step (c); and

(e) a step of selectively introducing nitrogen into the region to form said second field effect transistor on said semiconductor substrate and thereafter forming a gate insulation film on said semiconductor substrate, after said step (d).

20. A method for manufacturing a semiconductor integrated circuit device having a plurality of first field effect transistors constituting a memory cell of an SRAM and second field effect transistor other than them formed on a semiconductor substrate, which comprising:

(a) a step of forming a groove on said semiconductor substrate;

(b) a step of forming an isolation portion by burying an insulation film in said groove after said step of forming a groove;

(c) an impurity introduction step for selectively introducing a first impurity into a region to form at least one of said first field effect

transistors on said semiconductor substrate in order to set the threshold voltage of said at least one first field effect transistor among said plurality of first field effect transistors relatively higher than the threshold voltage of said second field effect transistor, after said step (b);

(d) an impurity introduction step for selectively introducing a second impurity into a region to form field effect transistors of the same conductivity type on said semiconductor substrate in order to set the threshold voltage of said second field effect transistor, after said step (b); and

(e) a step of selectively introducing nitrogen into the region to form said second field effect transistor on said semiconductor substrate and thereafter forming a gate insulation film on said semiconductor substrate after said step (d).

21. A semiconductor integrated circuit device according to claim 1,

wherein said second field effect transistors constitute a microprocessor.

22. A semiconductor integrated circuit device according to claim 2,

wherein said another field effect transistor constitutes a microprocessor.

23. A semiconductor integrated circuit device according to claim 3,

wherein said another field effect transistor constitutes a microprocessor.

24. A semiconductor integrated circuit device according to claim 4,

wherein said another field effect transistor constitutes a microprocessor.

25. A semiconductor integrated circuit device according to claim 5,

wherein said another field effect transistor constitutes a microprocessor.